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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,946	01/30/2002	Akira Goda	218447US2TTC	4857

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,946	GODA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 54-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 54 recites the phrases of "a memory cell having a first channel and a first gate insulating film ... the memory cell being sandwiched between the first shallow trench isolation regions ..." and "a transistor having a second channel and a second gate insulating ... the transistor being sandwiched between the second shallow trench isolation regions." This recitation carries an unclear meaning because it implies as if a memory cell and a transistor are distinctive structures, but actually meaning the same.

Claims 55-57 are dependent on the rejected base claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 48-50, 52, 54 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US 6326268), hereinafter Park in view of Yu et al. (US 6448606), hereinafter Yu.

Regarding claim 48, Fig. 7 of Park shows a semiconductor device comprising:

a semiconductor substrate (24);

a memory cell having a channel and a gate insulating film (30) formed on the semiconductor substrate, the gate insulating film comprising multiple layer films including a charge storage layer; and

shallow trench isolation regions (22) formed in trenches provided in the semiconductor substrate, the memory cell being sandwiched between the shallow trench isolation regions; and

wherein a film thickness of the gate insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation region is equal (col. 3, lines 17-25).

Fig. 7 of Park shows the most aspect of the instant invention except "the shallow trench isolation regions include concave portions on upper ends" and "the concave portions are formed above the charge storage layer." Fig. 5B of Yu shows "the shallow trench isolation regions (318B) include concave portions on upper ends" and "the concave portions are formed above the charge storage layer (306B)."

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yu into the device of Park in order to have "the shallow trench isolation regions include concave portions on upper ends" and "the concave portions are formed above the charge storage layer" for reduction of the device geometry.

Regarding claims 49 and 50, Fig. 7 of Park shows the gate insulating film (30) includes a first insulating film as the charge storage layer comprised of silicon and nitrogen as main constituent elements thereof and a second insulating film formed on the first insulating film, the second insulating film comprised of silicon and oxygen, and a third insulating film formed between the first insulating film and the semiconductor substrate, the third insulating film comprised of silicon and oxygen (ONO), and second (and third) insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal (col. 3, lines 52-58).

Regarding claim 52, Fig. 5B of Yu shows a gate electrode (308B) on the shallow trench isolation regions without interposition of the gate insulating film.

Regarding claim 54, insofar as understood, Fig. 7 of Park shows a semiconductor device comprising a semiconductor device comprising:

a semiconductor substrate (24);

a memory cell having a first channel and a first gate insulating film formed on the semiconductor substrate, the first gate insulating film (30) comprising multiple layer films including a charge storage layer; first shallow trench isolation regions (22) formed in trenches provided in the semiconductor substrate, the memory cell being sandwiched between the first shallow trench isolation regions; and

wherein a film thickness of the gate insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation region is equal (col. 3, lines 17-25).

Fig. 7 of Park shows the most aspect of the instant invention except "the shallow trench isolation regions include concave portions on upper ends" and "the concave portions are formed

above the charge storage layer." Fig. 5B of Yu shows "the shallow trench isolation regions (318B) include concave portions on upper ends" and "the concave portions are formed above the charge storage layer (306B)."

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yu into the device of Park in order to have "the shallow trench isolation regions include concave portions on upper ends" and "the concave portions are formed above the charge storage layer" for reduction of the device geometry.

Note that there is an array of memory cells identical to the ones shown in Fig. 7 while separated by the shallow trench isolation regions since Fig. 7 is only a portion of the entire memory structure.

Regarding claim 56, Fig. 7 of Park shows the gate insulating film (30) includes a first insulating film as the charge storage layer comprised of silicon and nitrogen as main constituent elements thereof and a second insulating film formed on the first insulating film, the second insulating film comprised of silicon and oxygen, and a third insulating film formed between the first insulating film and the semiconductor substrate, the third insulating film comprised of silicon and oxygen (ONO), and second (and third) insulating film at a central portion of the channel and at portions contacting with the shallow trench isolation regions are equal (col. 3, lines 52-58).

Claims 51, 53 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Yu as applied to claim 48 above, and further in view of Yu (US 6265293), hereinafter Yu-293.

Regarding claim 51, the combined teachings of Park and Yu show the most aspect of the instant invention except "a gate electrode on the gate insulating film, wherein a width of the gate insulating film in a direction of the channel is equal to a width of the gate electrode in the direction of the channel." Fig. 1 of Yu-293 shows "a gate electrode on the gate insulating film, wherein a width of the gate insulating film in a direction of the channel is equal to a width of the gate electrode in the direction of the channel."

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yu-293 into the device of Park and Yu in order to have a gate electrode on the gate insulating film, wherein a width of the gate insulating film in a direction of the channel is equal to a width of the gate electrode in the direction of the channel." to have the same size of the contact layer.

Regarding claim 53, the combined teachings of Park and Yu show the most aspect of the instant invention except "the gate electrode contains impurities, and wherein an impurity concentration of the gate electrode at a portion contacting with the gate insulating film is equal to an impurity concentration of the gate electrode at portions contacting with the shallow trench isolation regions." Fig. 1 of Yu-293 shows the gate electrode (40, 42) contains impurities (p-type or n-type), and wherein an impurity concentration of the gate electrode at a portion contacting with the gate insulating film is equal to an impurity concentration of the gate electrode at portions contacting with the shallow trench isolation regions.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yu-293 into the device of Park and Yu in order to have "the gate electrode contains impurities, and wherein an impurity concentration of the gate

electrode at a portion contacting with the gate insulating film is equal to an impurity concentration of the gate electrode at portions contacting with the shallow trench isolation regions" to reduce the surface resistance with the doped gate and constant doping concentration of the gate.

Regarding the aspect in which the impurity concentration of the gate electrode is equal at the portion contacting with the gate insulating film and at portions contacting with upper planes of the shallow trench isolation regions, it would be obvious that the impurity concentration of the gate electrode would be constant at the contacting portions of the gate insulating layer and the upper surfaces of the shallow trench isolation regions since the impurity is introduced on the continuous gate layer.

Regarding claim 57, the combined teachings of Park and Yu show the most aspect of the instant invention except "the memory cell has a first gate electrode and the transistor has a second gate electrode, and wherein the first gate electrode and the second gate electrode comprise polycrystalline silicon films, which are doped with impurities of conductivity types opposite to each other." Fig. 1 of Yu-293 shows a memory cell with a n-type gate (40) and an another memory cell with p-type gate (42).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yu-293 into the device of Park and Yu in order to have a memory cell with a n-type gate and an another memory cell with p-type gate to enhance the transistor performance.

Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Yu as applied to claim 54 above, and further in view of Hurley et al. (US 6265293), hereinafter Hurley.

Regarding claim 55, the combined teachings of Park and Yu show the most aspect of the instant invention except "heights, from a surface of the semiconductor substrate, of upper surfaces of the first trench isolation regions are higher than heights, from the surface of the semiconductor substrate, of upper surfaces of the second trench isolation regions." Fig. 3 of Hurley shows heights, from a surface of the semiconductor substrate (12), of upper surfaces of the first trench isolation regions are higher than heights, from the surface of the semiconductor substrate, of upper surfaces of the second trench isolation regions.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hurley into the device of Park and Yu in order to have "heights, from a surface of the semiconductor substrate, of upper surfaces of the first trench isolation regions are higher than heights, from the surface of the semiconductor substrate, of upper surfaces of the second trench isolation regions" to improve charge retention.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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